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PLL160M40M180nm

160MHz output frequency PLL

Key Parameters

- Output frequency: 160 MHz
- Reference frequency: 40 MHz
- Power consumption: 2.4 mW @ 1.8 V
- Cycle-cycle jitter: < 350 ps
  (60 ps_{RMS} @RT measured)
- Duty cycle: 35 % - 65 %
- Start-up time: < 1ms
- Supply voltage: 1.62 V – 1.98 V
- Temperature range: -40 °C – 125 °C

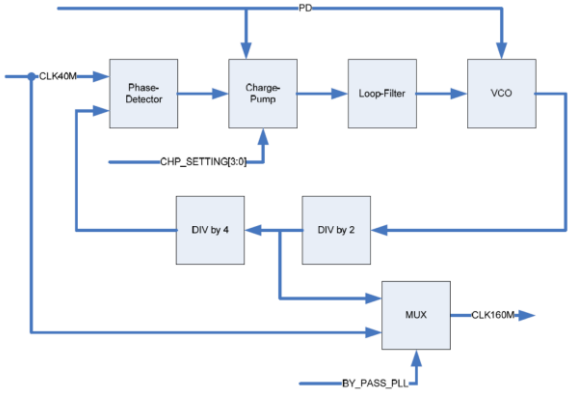

Fig. 1: IP-Level Block Diagram

General Description

The IP is a **complete PLL** including oscillator, loop filter, charge pump, phase detector and clock divider. The oscillator is realized as a differential ring oscillator, which enables a compact layout. The internal oscillator runs at 320 MHz.

The **loop filter** is completely **integrated** and, therefore, **no external components** are required. Decoupling capacitors are integrated for robust operation. The **overall size** of this IP block is **250 µm by 300 µm**.

The PLL is designed for a temperature range from **-40 °C up to 125 °C**. A voltage regulator for the **direct operation from 3.3 V or 5.0 V** is available on request.

The PLL is **silicon evaluated** using the **AMS C18** process. Measurement results are available from evaluation. One application of the IP is an industrial control ASIC.

Fraunhofer IIS provides a **documentation** and **support** for the IP integration. **Modifications, extensions and technology ports** of the IP are available on request.

Benefits

- Low design risk due to silicon evaluated design
- No external components due to integrated loop filter
- Improved testability of digital section due to bypass option
- Robust operation across full temperature range from -40 °C up to 125 °C

Deliverables

- GDSII data
- Simulation model
- Documentation
- Integration support

FACT SHEET

CONTACT

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