

More innovation through chip design

Bavarian Chip-Design-Center



BCDC Trainee Program



Position: Trainee in the field of Analog Chip Design or Test & Verification
Duration: 6 months, start: October 1, 2024
Location: Fraunhofer-Institut für Integrierte Schaltungen IIS, Am Wolfsmantel 33, 91058 Erlangen

What you do with us:

As a trainee, you will take part in a comprehensive introduction to analog chip design or test & verification and then work on real projects under the guidance of experienced engineers. You will gain hands-on experience in the design, simulation, layout and verification of analog integrated circuits, focusing on optimizing circuits for power, speed and area efficiency. In addition, you will have the opportunity to work in our collaborative work environment with other teams in the areas of layout and product management and learn about different aspects of semiconductor design.

What you need to bring:

- Master's degree in electrical engineering or related field of study such as physics, mathematics or medical engineering
- Team spirit, communication skills and the ability to work independently

Ideally

- Degree with a focus on microelectronics
- Knowledge of circuit technology
- Experience with design tools such as Cadence or Synopsys is an advantage.

Have we piqued your interest?

Then please contact us by email at yevgeniy.itskovych@iis.fraunhofer.de



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